WHAT IS CLAIMED IS:

1. A semiconductor device having an inductor on a semiconductor substrate, comprising a unit including:

an interlayer insulating film formed above said semiconductor substrate;

a spiral trench formed in said interlayer insulating film; and

an interconnection layer embedded within said spiral trench,

wherein said inductor is configured by a plurality of said units stacked up in a direction substantially perpendicular to a main surface of said semiconductor substrate, and

a plurality of said interconnection layers included in said plurality of units are arranged so as to be stacked up one after another in a direction perpendicular to the main surface of said semiconductor substrate, and have a substantially identical width.

2. The semiconductor device according to claim 1, wherein a width of said spiral trench is greater than a film thickness of said interlayer insulating film in which said spiral trench is formed.

3. The semiconductor device according to claim 1, wherein

said interconnection layer included in an uppermost layer unit of said plurality of units located at a position farthest from said semiconductor substrate is provided with a drawing electrode portion which can draw current from said inductor;

said drawing electrode portion has a protrusion protruding beyond an outermost edge of said interconnection layer included in said unit below the uppermost layer unit, in a direction perpendicular to the main surface of said interlayer insulating film; and

a plug is formed from an upper side of said protrusion so as to connect with said protrusion.

4. A method of manufacturing the semiconductor device according

to claim 1,

said semiconductor device being provided with a logic circuit region which is a region different from a region where said inductor is formed, and in which a logic circuit is formed, wherein said logic circuit region is provided with a logic circuit interconnection layer which constitutes said logic circuit;

the step of forming said spiral trench being performed together with a part of the step of forming a trench for the logic circuit interconnection layer in which said logic circuit interconnection layer is embedded; and

the step of forming the trench for said logic circuit interconnection layer including the steps of

forming a first trench portion by performing said part of the step to said interlayer insulating film, and

etching the interlayer insulating film in which the first trench portion is formed after the step of forming the first trench portion, to form a second trench portion which has a width greater than that of the first trench portion, over the first trench portion,

wherein, in the step of forming the second trench portion, etching to form said second trench portion is performed with said spiral trench covered with a mask.